

A Review of Low Power High Speed Flash ADC Design Techniques

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ABSTRACT: The Data converters are essential interface circuits between the analog world that people live in and the digital processors that people live with. Linearity, which often is a tradeoff against other performance criteria, is one of the major performance demands from applications for both Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC). There are many types of ADC's available such as pipeline ADC, successive approximation ADC, delta sigma ADC etc. In present day CMOS technology the flash ADC is composed by utilizing the dynamic method, it reduces the power and delay. A flash ADC is extremely valuable for fastest speed operations when it is compared with the other ADC architectures. Comparator and Encoder are vital part of flash ADC. This paper presents review of Efficient Low Power High Speed Flash ADC Techniques.

KEYWORDS: ADC, Flash ADC, Resolution, Conversion rate, Comparator, Conversion speed, Encoder

I. INTRODUCTION

Mixed signals are wide spread in many applications for example in Audio video etc. Digital receivers for high bit rate communications are spurring on the conversion rate of Analog to- Digital Converters (ADCs). With phenomenal growth of modern communications and signal processing systems, handheld wireless computers and portable electronics are becoming increasingly popular. ADCs are becoming part of System-On-Chip (SOC) instead of a standalone circuit for data converter. The average power consumption and the speed in these applications has become the most critical design concern. To limit energy in a reasonable size battery, minimum power dissipation in the mixed signal integrated circuits is necessary. Although the Flash type ADC design has been widely defined for these applications, and has different architectures, resolutions, sampling rates, power consumptions and a range of operating temperatures. These features available in a Flash ADC are of prime importance. A high trade-off is found among these parameters. The power dissipation increases with the increase in speed and resolution. This results in limitations for Flash ADC at higher resolutions.

II. FLASH ADC WITH QV COMPARATOR

The ADC using the proposed QV comparator is a full flash type. As shown in Figure 1 the ADC consists of four blocks: comparator, gain booster, '01' generator, and a fat tree encoder. An analog input voltage, V_{in} , is connected to each QV comparator at the same time. The V_{in} is compared with an internal reference voltage (V_{ref}) in each comparator. To obtain a larger gain, a gain booster is connected to each comparator output. Since the output of the gain booster stage is a thermometer code, an encoder is needed to change the thermometer code to a binary code. This encoding process has two steps. The first step is converting the thermometer code to the 1-out-of-n code with simple XOR logic, which is implemented with NAND gates.

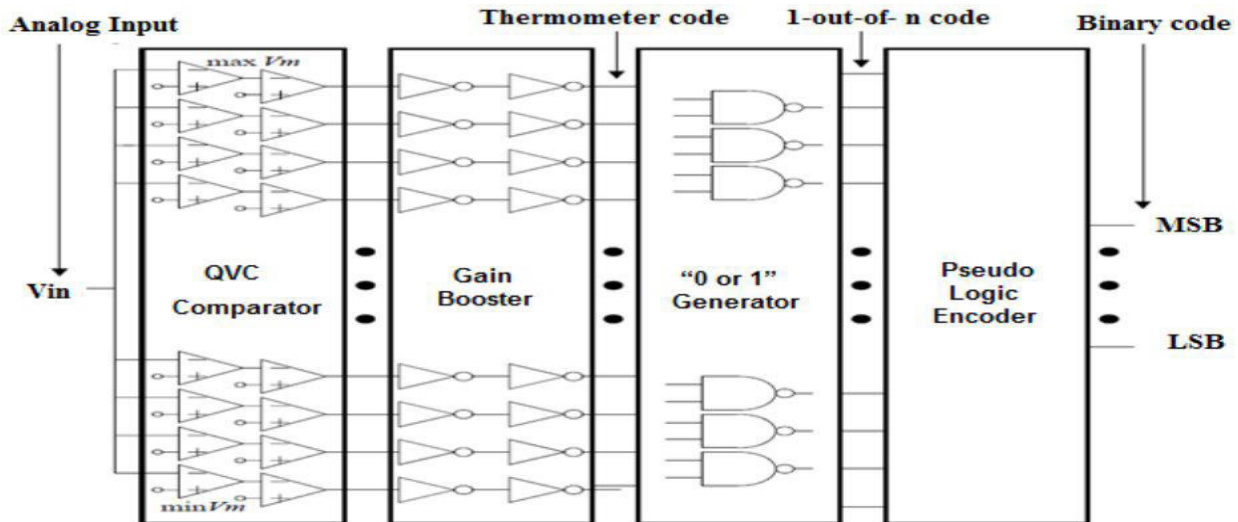


Figure.1 ADC architecture using the QVC comparator

Encoder is used to change the 1-out-of-n code into a binary code. A new digital encoder network called the Pseudo-dynamic NMOS encoder is used in the QVC based architecture of flash ADC. The Pseudo dynamic NMOS encoder outperforms all of the existing encoding networks. The new encoding network offers high data conversion rate with low power consumption.

III LITERATURE REVIEW

This paper gives survey on various techniques of Flash ADC design. Researchers have implemented flash ADC with different number of bits and different CMOS technologies

Jincheol Yoo et al., [1] this paper presents a new voltage comparator design called Quantum Voltage (QV) comparator for the next generation deep sub-micron low voltage CMOS flash A/D converter (ADC). The new QV comparator has been designed and simulated to verify the low voltage operation. Both the 6-bit QVC flash ADC and the 8-bit QVC flash ADC are correctly operating with high speed and low power consumption. The simulation results with a 0.7 V power supply shows that the QV comparator has a great advantage in power consumption and noise rejection.

Geetanjali Sharma et al., [2] the comparative analysis, we have chalked out the best and worst styles based upon their estimated power consumption, PDP and the area calculation based upon the number of transistors. Seven different approaches to implement a 2 bit magnitude comparator have been discussed below. The best magnitude comparator using Hybrid PTLI CMOS logic style, derived from this analysis has been proposed in this paper.

Megha R and Pradeepkumar K A [3] A 4-bit CMOS based flash ADC is presenting, which uses reduced comparator and multiplexer based architecture. Here both the analog and the digital parts of the proposed ADC are completely modified. This architecture uses only 4 comparators for a 4 bit ADC. This 4-bit ADC is designed and simulated in Hspice with 1.2 V supply voltage.

Ranam Sireesha and Abhishek Kumar [4]The design 4 Bit flash ADC with Using TIQ Technique comparator .TIQ Comparator Compared Input signal with linearity generated switching and produce thermometer code. An efficient thermometer to binary converter has been design using transmission gate based 2:1 multiplexer .This design operated at 800 mv of input frequency 1k Hz .

Liyaqat Nazir et al., [5] new digital encoder network called the Pseudo- dynamic NMOS encoder is proposed to be used in the proposed TIQ based architecture of flash ADC. The 4 Bit Flash ADC is designed using Pseudo dynamic NMOS encoder which out performs all of the existing encoding networks. The new encoding network offers high data conversion at rate of 7 GS/s with low power consumption.

A. Manikandan et al., [6] Comparator Designed Using Current Comparison Based Domino Logic. This Simulation results of 64 bit comparator designed using a 22nm high performance predictive technology model demonstrate 51% power reduction compared to a standard domino circuits for 64 bit comparator consumption and also the delay of the circuit simulation

Meghana Kulkarni et al., [18] proposed a FLASH ADC design based on the use of a Quantized Differential comparator. The design has been implemented using TSMC 180nm Technology at MOSIS. The work is an extension of TIQ method which uses systematic sizing of devices in a Conventional CMOS Inverter. The designed ADC has characteristics like Resolution of 6-bit, Power Dissipation of 36.98mW at a power supply of 1.8V.

TABLE I
RESULT ANALYSIS

The Table 1 shows Result and Analysis's of different Architecture and Techniques for the following Survey Papers.

Author	Architecture	Resolution	Input voltage	Design Techniques	Simulation Tool and Technology file	Improved Parameter
Jincheol Yoo et.al [1]	6 Bit and 8 Bit FLASH ADC	6 Bit and 8 Bit	0.7 V	Comparator designed using QVC Technique	Cadence Tool	2.7 GSPS Sampling rate.
Geetanjali Sharma et.al [2]	2 bit Comparator	2 bit	0.6 -1.2 V	Comparator designed using Hybrid PTLI CMOS Technique	Tanner EDA Tool(45 nm)	Low power consumption.
Megha R and Pradeepkumar K A[3]	4 Bit FLASH ADC	4 Bit	1.2 V	Encoder designed using multiplexer Technique	HSpice	Power Dissipation- 11.5 mW, 2. GSPS Sampling rate.
Ranam Sireesha and Abhishek Kumar [4]	4 Bit FLASH ADC	4 Bit	0.8 V	Comparator designed using TIQ Technique	Cadence tool (120 nm)	Power Dissipation- 14.08uW and delay 200 us.
Liyaqat Nazir et.al [5]	4 Bit FLASH ADC	4 Bit	1.2 V	Encoder designed using Pseudo dynamic technique	Cadence tool (90 nm)	Speed 7 GS/s.
A. Manikandan et.al [6]	64 bit Comparator	64 bit	0.5 V	Comparator Designed Using Current Comparison Based Domino Logic	Cadence Tool (22 nm)	Reduces Area and Power Consumption.
Suman Biswas et.al [7]	4 Bit FLASH ADC	4 Bit	1.8 V	Comparator designed using low offset dynamic Technique	Cadence Tool (180 nm)	Power Dissipation- 1.5mW.
Taninki Sai Lakshmi and Avireni Srinivasulu [8]	5 Bit FLASH ADC	5 Bit	1.2V	Thermometer code to Binary code through using	Cadence Tool (180 nm)	Sampling Frequency 5 GS/s.

				(DCVSL) Technique		
Anshul Pathak and Shyam Akashe [9]	3 Bit FLASH ADC	3 Bit	0.7V	Flash ADC designed using the Stacked Power gating Technique	Cadence Tool (45 nm)	Reduces Leakage power.
Vijay V. Chakole et.al [10]	4-bit FLASH ADC	4-Bit	1.8V	Encoder designed using MUX based Technique	TANNER tool (180nm)	Input Frequency-10MHz, SNR-25.5DB.
Anjuli et.al [11]	2-bit Comparator	2-Bit	0.6 -1.4 V	Comparator designed using TG,PTL Technology	Tanner EDA (90 nm)	Pseudo NMOS provides least delay amongst all, PTL provides less PDP, Output Swing is better in CMOS and Transmission Gate design.
Kalpna Chaudhary et.al [12]	3-bit FLASH ADC	3-Bit	0.9V	Comparator designed using TIQ technique	Tanner EDA (90 nm)	Leakage Power-18nW, Average Power Consumed-870µW.
Sunghyun Park et.al [13]	4 bit flash ADC	4 bit	1.8 V	Designed using Comparator Core With Inductors Technique	Tanner EDA (180 nm)	Power consumption-78 mW.
Mingzhen Wang et.al [14]	4 bit flash ADC	4 bit	1.2 V	Comparator designed using Timed Digital with dynamic offset Technique	Tanner EDA (90 nm)	Power consumption-1.35 m Conversion rate-2.5GHz.
Mamta Gurjar et.al [15]	3 bit flash ADC	3 bit	0.7 V	TIQ technique	Cadence Tool (45 nm)	Speed-5.3 Gs/s Bandwidth-16.65 MHz.
Gulrej Ahmed et.al [16]	6 bit flash ADC	6 bit	1.2 V	Comparator designed using Variable Switching Voltage CMOS Technique	Cadence Tool (65 nm)	Speed-1 GHz.
S. S. Khot [17]	6 bit flash ADC	6 bit	2.5 V - 3.3 V	Comparator designed using TIQ technique	Cadence Tool (250 nm)	Speed- 500- 565msps.
Meghana Kulkarni et.al [18]	6-bit FLASH ADC	6-Bit	1.8V	Comparator designed using Quantized Differential Technique	TSMC (180 nm)	Power Dissipation-36.98mW.

IV. CONCLUSIONS

In this paper different methods of designing flash ADC are examined. Comparator and encoder is vital part of designing Flash ADC. Different methods of designing Flash converter by various authors are compared for performance parameters like power consumption, conversion speed, gain, bandwidth, accuracy, and different technologies employed for obtaining better results.

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